Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A data processor comprising:

a random access memory;

a processing unit for carrying out data processing while accessing said random access memory; and

a conversion unit for converting data so that the number of bits having a predetermined value out of said data is at least a predetermined number for output to said random access memory when said processing unit writes said data into said random access memory.

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2. (Currently Amended) The data processor according to claim 1, wherein said conversion unit includes

a detection circuit for detecting, when said processing unit writes data into said random access memory, whether the number of bits having a first value out of said data is at least the number of bits having a second value differing from said first value to set a flag,

a first inversion circuit for inverting said data for output, and

a first select circuit responsive to the flag set by said detection circuit to selectively provide said data and said inverted data output from said first inversion circuit to said random access memory.

3. (Currently Amended) The data processor according to claim 2, further comprising:

a second inversion circuit for inverting data output from said random access memory for output; and

a second select circuit responsive to said flag to selectively provide data output from said random access memory and said inverted data output from said second inversion circuit to said processing unit when said processing unit reads out data from said random access memory.

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4. (Currently Amended) A data processor comprising:

a random access memory;

a processing unit for carrying out data processing while accessing said random access memory;

a first retain circuit for storing previous data output by said processing unit; and

a subtracter for taking a difference between the previous data stored in said retain circuit and current data output by said processing unit when said processing unit writes data into said random access memory.

5. (Currently Amended) The data processor according to claim 4, further comprising a variable-length coder for applying variable-length coding on difference data output from said subtracter for output to said random access memory.

6. (Currently Amended) The data processor according to claim 4, further comprising:

a first detection circuit for detecting a data write timing of a predetermined period including the write timing of the first data out of the data write timing into said random access memory by said processing unit; and

a first selector for selecting data output from said processing unit at the timing detected by said first detection circuit for output, and selecting difference data output from said subtracter at a timing other than the timing detected by said first detection circuit for output.

7. (Currently Amended) The data processor according to claim 4, further comprising:

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a second retain circuit for storing previous data output to said processing unit; and

an adder for adding difference data output from said random access memory [[and]] to said previous data stored in said second retain circuit.

8. (Currently Amended) The data processor according to claim 7, further comprising a variable-length decoder for applying variable-length decoding on variable-length coded difference data output from said random access memory to output the decoded data to said adder.

9. (Currently Amended) The data processor according to claim 7, further comprising:

a second detection circuit for detecting a data readout timing of a predetermined period including the readout timing of the first data among the data readout timing by said processing unit; and

a second selector for selecting data output from said random access memory at the timing detected by said second detection circuit for output, and selecting the data output from said adder at a timing other than said timing detected by said second detection circuit for output.

10. (Original) A data processing method of carrying out data processing while accessing a random access memory, said method comprising the steps of:

converting write data so that the number of bits having a predetermined value out of said write data is at least a predetermined value; and

A1 writing said converted write data to said random access memory.

11. (Original) The data processing method according to claim 10, wherein said step of converting write data includes the steps of

detecting whether the number of bits having a first value out of said write data is at least the number of bits having a second value differing from said first value to set a flag,

inverting said write data for output, and

selectively providing said write data and said inverted write data to said random access memory according to said set flag.

12. (Original) The data processing method according to claim 11, further comprising the steps of:

inverting data read out from said random access memory for output; and

selectively providing the data read out from said random access memory and said inverted read out data based on said set flag.